IN THE CLAIMS:

Please amend the claims as set forth below.

1-60. (Cancelled)

61. (Currently Amended) A processor comprising:

a register file including a plurality of registers; and

an execution core coupled to the register file, wherein the execution core is configured to: (i) use a value of a register address field of an instruction to select a least significant portion of one of the plurality of registers responsive to detecting a prefix field in the instruction, wherein each value encodable in the register address field results in a selection of the least significant portion of a respective one of the plurality of registers; and (ii) use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register.

62. (Previously presented) The processor as recited in claim 61 wherein the prefix field is a prefix byte.

63. (Previously presented) The processor as recited in claim 61 wherein the instruction specifies a one byte operand size.

64. (Previously presented) The processor as recited in claim 63 wherein the least significant portion and the second least significant portion are each a byte.

65. (Currently Amended) An apparatus comprising:

one or more storage locations corresponding to a plurality of registers; and

a processor coupled to the one or more storage locations, wherein the processor is operable to: (i) use a value of a register address field of an instruction to select a least significant portion of one of the plurality of registers responsive to detecting a prefix field in the instruction, wherein each value encodable in the register address field results in a selection of the least significant portion of a respective one of the plurality of registers; and (ii) use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register.

66. (Previously presented) The apparatus as recited in claim 65 wherein the prefix field is a prefix byte.

67. (Previously presented) The apparatus as recited in claim 65 wherein the instruction specifies a one byte operand size.

68. (Previously presented) The processor as recited in claim 67 wherein the least significant portion and the second least significant portion are each a byte.

69. (Currently Amended) A method comprising:

responsive to detecting a prefix field in an instruction that also includes a register address field, selecting a least significant portion of one of a plurality of registers dependent on a value of the register address field, wherein each value encodable in the register address field maps to a different one of the plurality of registers; and

responsive to detecting a lack of the prefix field in the instruction, selecting either a least significant portion or a second least significant portion of one of a subset of the plurality of registers dependent on the value of the register address field, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register.

70. (Previously presented) The method as recited in claim 69 wherein the prefix field is a prefix byte.

71. (Previously presented) The method as recited in claim 69 wherein the instruction specifies a one byte operand size.

72. (Previously presented) The method as recited in claim 71 wherein the least significant portion and the second least significant portion are each a byte.

73. (Currently Amended) A computer system comprising:

a processor comprising a register file including a plurality of registers, wherein the processor is configured to: (i) use a value of a register address field of an instruction to select a least significant portion of one of the plurality of registers responsive to detecting a prefix field in the instruction, wherein each value encodable in the register address field results in a selection of the least significant portion of a respective one of the plurality of registers; and (ii) use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register; and

a peripheral device configured to communicate between the computer system and another computer system.

74. (Previously presented) The computer system as recited in claim 73 wherein the prefix field is a prefix byte.

75. (Previously presented) The computer system as recited in claim 73 wherein the

instruction specifies a one byte operand size.

76. (Previously presented) The computer system as recited in claim 73 wherein the least significant portion and the second least significant portion are each a byte.

77. (Previously presented) The computer system as recited in claim 73 wherein the peripheral device comprises a modem.

78. (Previously presented) The computer system as recited in claim 73 wherein the peripheral device comprises a network interface device.

79. (Currently Amended) The computer system as recited in claim 73 further comprising a second processor comprising a register file including a plurality of registers, wherein the second processor is configured to: (i) use a value of a register address field of an instruction to select a least significant portion of one of the plurality of registers responsive to detecting a prefix field in the instruction, wherein each value encodable in the register address field results in a selection of the least significant portion of a respective one of the plurality of registers; and (ii) use the value of the register address field to select one of either a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers, wherein a first value encodable in the register address field results in the selection of the least significant portion of a first register of the plurality of registers if the instruction includes the prefix field, and wherein the first value results in the selection of the second least significant portion of a second register of the plurality of registers if the instruction does not include the prefix field, and wherein the second register is different from the first register.

80. (Previously presented) The computer system as recited in claim 73 further comprising an audio device.